IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants: Desmicht et al. Group Art Unit: 2432

Serial No.: 10/536,732 Examiner: Okeke, Izunna

Filed: May 27, 2005 Confirmation No.: 4315

For: CHIP INTEGRATED PROTECTION MEANS

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Sir/Madam:

This brief is in furtherance of Applicants' Notice of Appeal filed on November 5, 2009, appealing the decision of the Examiner dated August 5, 2009 finally rejecting claims 1, 3 and 5-13.

I. Real Party in Interest

The real party in interest in this appeal is NXP B.V., High Tech Campus 60, 5656 AG Eindhoven, The Netherlands.

II. Related Appeals and Interferences

There are currently no related appeals or interference proceedings in progress that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the present Appeal.

III. Status of Claims

Claims 1-11 were originally filed on May 27, 2005. In a preliminary amendment filed on May 27, 2005, claims 3, 4, 7, 9 and 11 were amended. In response to the Office Action of May 7, 2008, claims 1, 9 and 11 were amended, and claim 2 was canceled. In response to the Office Action of September 12, 2008, claims 1 and 5-11 were amended, claim 4 was canceled, and new claims 12 and 13 were added. Claims 1, 3 and 5-13 stand finally rejected and form the subject matter of the present appeal.

Claims 1, 3 and 5-12 are rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Pat. Pub. No. 2003/0014653 ("Moller et al."). Claim 13 is rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Moller et al. in view of U.S. Pat. No. 6,118,870 ("Boyle et al.").

This Appeal is made with regard to pending claims 1, 3 and 5-13.

IV. Status of Amendments

No amendments were filed subsequent to final rejection.

V. Summary of Claimed Subject Matter

The claimed invention includes a chip for processing a content, a device intended to recover a content from a media and to process the content, and a method for obtaining a protected chip including at least a microprocessor. (See lines 2-6 on page 1 and lines 18-31 on page 3 of the Specification).

According to an embodiment, as recited in the independent claim 1, a chip (CHP) for processing a content, comprising at least a microprocessor (MP) (See Figs. 2-4, line 34 on page 4, lines 1-5 and 26-29 on page 5, and lines 17-23 on page 12 of the Specification), characterized in that said chip (CHP) includes an integrated non-volatile programmable memory (NVM, NVMS) for storing protection data (ADA) and protected data (PDA) (See Figs. 2-4, line 34 on page 4, lines 1-5, 15-19, and 26-29 on page 5, lines 15-19 on page 8, and lines 17-23 on page 12 of the Specification), said protection data (ADA) being intended to define a protection level for authorizing/denying access to said protected data (PDA) by said microprocessor (MP) while a program (PRO) is executed (See Figs. 2-4, line 34 on page 4, lines 1-5 and 26-29 on page 5, and lines 20-24 on page 8 of the Specification), wherein said protection data is only modifiable so as to increase said protection level and said protected data includes data to activate/deactivate an optional feature of the chip (See line 30 on page 5-line 13 on page 8 of the Specification).

According to another embodiment, as recited in the independent claim 9, a device (DEV) intended to recover a content from a media (VCM) and to process said content (See Figs. 1-4, lines 7-12 on page 4, lines 24-27 on page 9, and lines 17-23 on page 12 of the Specification), said device (DEV) including a connection (BUS) to said media and a chip (CHP) (See Figs. 2-4, lines 13-18 on page 4, and lines 7-9 on page 16 of the Specification), wherein the chip (CHP) comprising: at least a microprocessor (MP) (See Figs. 2-4, line 34 on page 4, lines 1-5 and 26-29 on page 5, and lines 17-23 on page 12 of the Specification); and an integrated non-volatile programmable memory (NVM, NVMS) for storing protection data (ADA) and protected data (PDA) (See Figs. 2-4, line 34 on page 4, lines 1-5, 15-19, and

26-29 on page 5, lines 15-19 on page 8 and lines 17-23 on page 12 of the Specification), said protection data (ADA) being intended to define a protection level for authorizing/denying access to said protected data (PDA) by said microprocessor (MP) while a program (PRO) is executed (See Figs. 2-4, line 34 on page 4, lines 1-5 and 26-29 on page 5, and lines 20-24 on page 8 of the Specification), wherein said protection data is only modifiable so as to increase said protection level and said protected data includes data to activate/deactivate an optional feature of the chip (See line 30 on page 5-line 13 on page 8 of the Specification).

According to another embodiment, as recited in the independent claim 11, a method for obtaining a protected chip (CHP) including at least a microprocessor (MP) (See Figs. 2-4, line 34 on page 4, lines 1-5 and 26-29 on page 5, and lines 17-23 on page 12 of the Specification), said method using a chip (CHP), said method including: using at least an authorized access to modify protected data (PDA) in an integrated non-volatile memory (NVM, NVMS) (See Figs. 2-4, line 34 on page 4, lines 1-5, 15-19, and 26-29 on page 5, lines 15-19 on page 8, and lines 17-23 on page 12 of the Specification), protecting the access to said protected data (PDA) in said integrated non-volatile memory (NVM, NVMS) by modifying protection data (ADA) in order to deny said access (See Figs. 2-4, line 34 on page 4, lines 1-5, 15-19, and 26-29 on page 5, lines 15-19 on page 8 and lines 17-23 on page 12 of the Specification), wherein said protection data (ADA) being intended to define a protection level for authorizing/denying access to said protected data (PDA) by said microprocessor (MP) while a program (PRO) is executed (See Figs. 2-4, line 34 on page 4, lines 1-5 and 26-29 on page 5, and lines 20-24 on page 8 of the Specification), wherein said protection data (ADA) is only modifiable so as to increase said protection level and said protected data (PDA) includes data to activate/deactivate an optional feature of the chip (CHP) (See line 30 on page 5-line 13 on page 8 of the Specification).

VI. Grounds of Rejection to be Reviewed on Appeal

Whether claims 1, 3 and 5-12 are anticipated under 35 U.S.C. §102(e) by Moller et al.

Whether claim 13 is unpatentable under 35 U.S.C. §103(a) over Moller et al. in view of Boyle et al.

VII. Argument

In the Final Office Action of August 5, 2009, the Examiner rejected claims 1, 3 and 5-12 under 35 U.S.C. §102(e) over Moller et al. Additionally, the Examiner rejected claim 13 under 35 U.S.C. §103(a) over Moller et al. in view of Boyle et al. However, the reference Moller et al. cited by the Examiner fails to disclose all of the limitations of independent claims 1, 9 and 11, as explained below. Thus, independent claims 1, 9 and 11 and dependent claims 3, 5-8, 10 and 12 are not anticipated by Moller et al. Additionally, dependent claim 13 is not unpatentable under 35 U.S.C. §103(a) over Moller et al. in view of Boyle et al., as explained below.

A. Rejection of Claims 1, 3 and 5-12 Under 35 U.S.C. §102(e)

Independent claims 1, 9 and 11 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Moller et al. However, the reference Moller et al. cited by the Examiner fails to disclose all of the limitations of independent claims 1, 9 and 11. Thus, independent claims 1, 9 and 11 are not anticipated by Moller et al.

Independent claim 1 recites in part "*said protection data is only modifiable so as to increase said protection level*," which is not disclosed by Moller et al. Thus, Applicants respectfully assert that claim 1 is not anticipated by Moller et al.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

On page 2 of the Final Office Action, the Examiner states that "Moller describes the protection data (Key 1, Key 2) which are passwords which must be present for the decryption of the protected data." Additionally, on page 2 of the Final Office Action, the Examiner states that "the protection data is (Key 1, Key 2) for protecting access to the data..." Furthermore, on page 2 of the Final Office Action, the Examiner states that "[t]he 1 and 0 bits which enable and disable the external interface in Moller's inventor are not the protection data but are part of the protected data in the PCR." Thus, the Examiner has equated passwords, Key 1 and Key 2, described in Moller et al. with the claimed "*protection data*" and the 1 and 0 bits described in Moller et al. with the claimed "*protected data.*"

Applicants respectfully assert that Moller et al. fails to disclose that the passwords are "*only modifiable so as to increase said protection level*," (emphasis added), as recited in claim 1. Thus, Applicants respectfully assert that Moller et al. fails to disclose that "*said protection data is only modifiable so as to increase said protection level*," (emphasis added), as recited in claim 1.

Moller et al. discloses that during reprogramming, an existing password for decryption of received data is replaced by a new password in the second and third memory blocks (5), (6). (See Fig. 1 and paragraph [0025] of Moller et al.). Moller et al. also discloses that memory blocks (4), (5), (6) are associated with the second memory portion (3) so that a change of the access authorization or the password is possible by reprogramming or updating. (See paragraph [0027] of Moller et al.). That is, Moller et al. discloses that the passwords can be replaced. However, Moller et al. fails to disclose that the passwords are "*only modifiable so as to increase said protection level*," (emphasis added), as recited in claim 1. Thus, Moller et al. fails to disclose the limitation of "*said protection data is only*

modifiable so as to increase said protection level," as recited in claim 1. Consequently, independent claim 1 is not anticipated by Moller et al.

Applicants note that, in the Advisory Action of September 28, 2009, the Examiner apparently uses the access control bit (0 or 1) to assert that Moller et al. discloses the claimed limitation of "*said protection data is only modifiable so as to increase said protection level*." However, as noted above, the Examiner has already equated the 1 and 0 bits described in Moller et al. with the claimed "*protected data,*" not the claimed "*protection data*." Specifically, the Examiner has stated on page 2 of the Final Office Action that "[t]he 1 and 0 bits which enable and disable the external interface in Moller's inventor are not the protection data but are part of the protected data in the PCR." Thus, the 1 and 0 bits described in Moller et al. cannot now be equated to the claimed "*protection data.*"

The above remarks are also applicable to independent claims 9 and 11, which include limitations similar to those of independent claim 1. As such, the reference Moller et al. cited by the Examiner also failed to disclose all of the limitations of independent claims 9 and 11. Thus, independent claims 9 and 11 are also not anticipated by Moller et al.

Claims 3, 5-8 and 12 depend from and incorporate all of the limitations of independent claim 1. Thus, Applicants respectfully assert that claims 3, 5-8 and 12 are allowable at least based on an allowable claim 1. Additionally, claim 10 depends from and incorporates all of the limitations of independent claim 9. Thus, Applicants respectfully assert that claim 10 is allowable at least based on an allowable claim 9.

B. Rejection of Dependent Claim 13 Under 35 U.S.C. §103(a)

Dependent claim 13 depends on independent claim 1. As such, dependent claim 13 includes all the limitations of the base claim 1. Because the reference Moller et al. cited by the Examiner fails to disclose all of the limitations of

independent claim 1, the Examiner has failed to establish a *prima facie* case of obviousness for dependent claim 13 using the cited references of Moller et al. and Boyle et al. As a result, dependent claim 13 is patentable over Moller et al. in view of Boyle et al.

SUMMARY

The reference Moller et al. cited by the Examiner fails to disclose all of the limitations of independent claims 1, 9 and 11. Thus, independent claims 1, 9 and 11 are not anticipated by Moller et al. Dependent claims 3, 5-8, 10 and 12 are patentable for at least the same reasons as their base claims 1 and 9. Additionally, because dependent claim 13 depends on independent claim 1 and includes all the limitations of independent claim 1, the Examiner has failed to establish a *prima facie* case of obviousness for dependent claim 13 using the cited references of Moller et al. and Boyle et al. As a result, dependent claim 13 is patentable over Moller et al. in view of Boyle et al.

For all the foregoing reasons, it is earnestly and respectfully requested that the Board of Patent Appeals and Interferences reverse the rejections of the Examiner regarding claims 1, 3 and 5-13, so that this case may be allowed and pass to issue in a timely manner.

Respectfully submitted,
Desmicht et al.

Date: January 5, 2010

By: /thomas h. ham/
Thomas H. Ham
Registration No. 43,654
Telephone: (925) 249-1300

VIII. Claims Appendix

1. A chip for processing a content, comprising at least a microprocessor, characterized in that said chip includes an integrated non-volatile programmable memory for storing protection data and protected data, said protection data being intended to define a protection level for authorizing/denying access to said protected data by said microprocessor while a program is executed, wherein said protection data is only modifiable so as to increase said protection level and said protected data includes data to activate/deactivate an optional feature of the chip.

3. A chip according to Claim 1, wherein said protection data includes a password, said access being authorized/denied through a password check.

5. A chip according to Claim 1, wherein said optional feature is a connection to an external device for downloading a program and/or data from said external device.

6. A chip according to Claim 1, wherein said protected data includes data to activate/deactivate an external boot program for said microprocessor, said external boot program including instructions for downloading a new boot program for said microprocessor from an external memory.

7. A chip according to Claim 1, wherein said protection data includes a value defining an address limit from which the data stored at said memory are protected data and access to such protected data is denied.

8. A chip according to Claim 7, wherein said protected data includes programs and data operating a conditional-access dedicated microprocessor.

9. A device intended to recover a content from a media and to process said content, said device including a connection to said media and a chip, wherein the chip comprising:

at least a microprocessor; and

an integrated non-volatile programmable memory for storing protection data and protected data, said protection data being intended to define a protection level for authorizing/denying access to said protected data by said microprocessor while a program is executed, wherein said protection data is only modifiable so as to increase said protection level and said protected data includes data to activate/deactivate an optional feature of the chip.

10. A device as claimed in Claim 9, wherein the device is intended to process encrypted video/audio data.

11. A method for obtaining a protected chip including at least a microprocessor, said method using a chip, said method including:

using at least an authorized access to modify protected data in an integrated non-volatile memory,

protecting the access to said protected data in said integrated non-volatile memory by modifying protection data in order to deny said access, wherein said protection data being intended to define a protection level for authorizing/denying

access to said protected data by said microprocessor while a program is executed, wherein said protection data is only modifiable so as to increase said protection level and said protected data includes data to activate/deactivate an optional feature of the chip.

12. A chip according to Claim 1 further comprising a random logic coupled between said integrated non-volatile programmable memory and a connection bus of said microprocessor.

13. A chip according to Claim 1, wherein said microprocessor is a processor having a MIPS instruction set.

IX. Evidence Appendix

NONE

X. Related Proceedings Appendix

NONE